Limit Cycle Suppression Technique Using Random Signal In Delta-Sigma DA Modulator

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Research Objective

Objective

- **Development of high linear & high resolution ΔΣ DAC**

Studies

- **Limit cycle suppression using random signal at quantizer input.**

Outline

- Research Background
- Proposed Circuit
- Simulation Configuration & Results
- Conclusion

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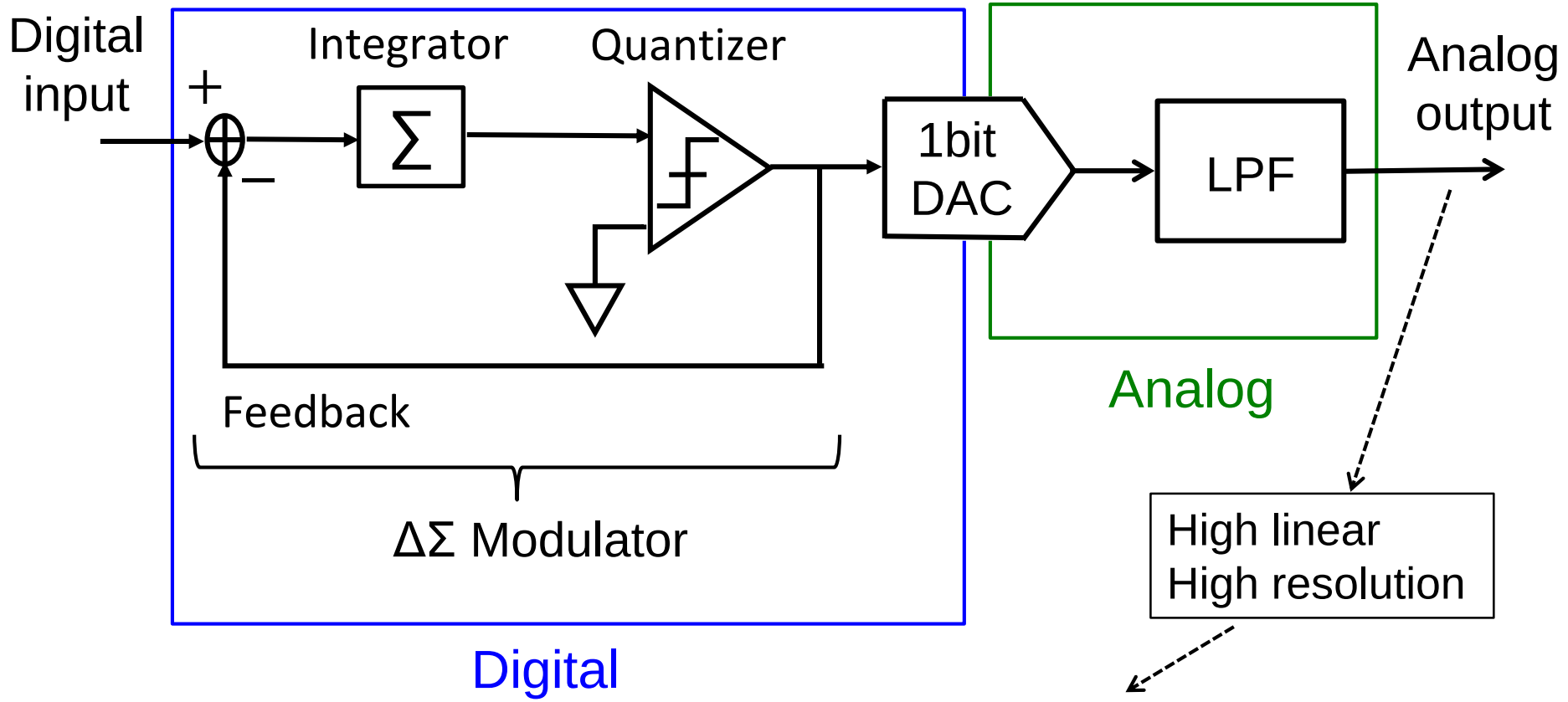
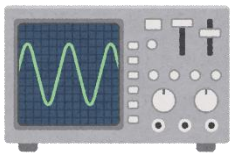
ΔΣ DA Converter



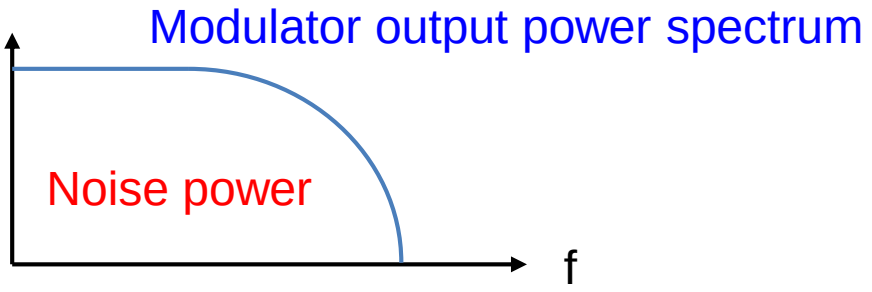
＜Usage＞



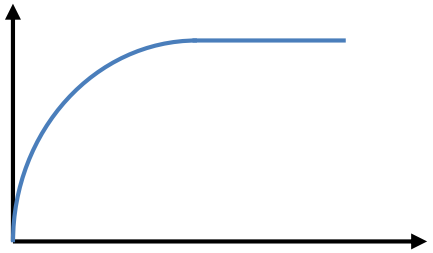
- Measurement
- Audio system
- Satellite communication

Modulator type

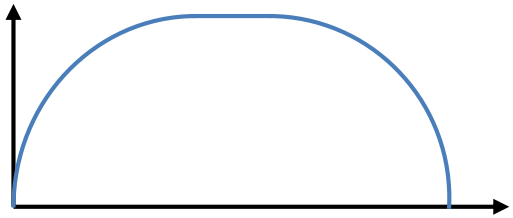
(1) low-pass (LP) type



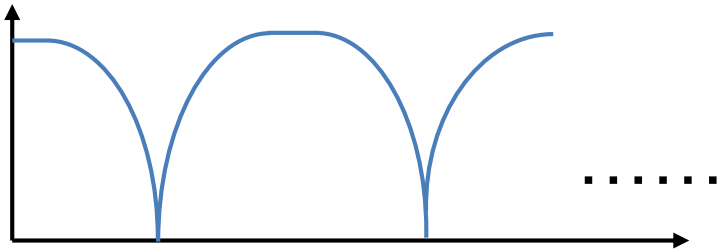
(2) high-pass (HP) type



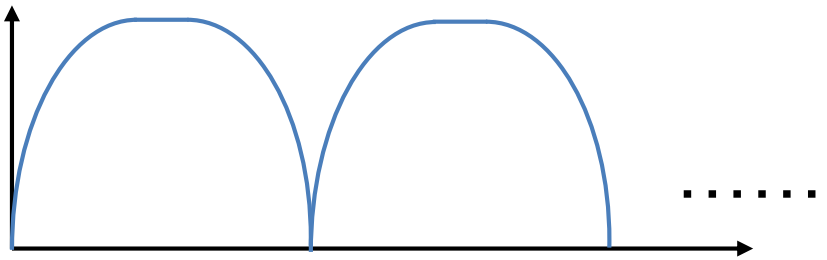
(3) band-pass (BP) type



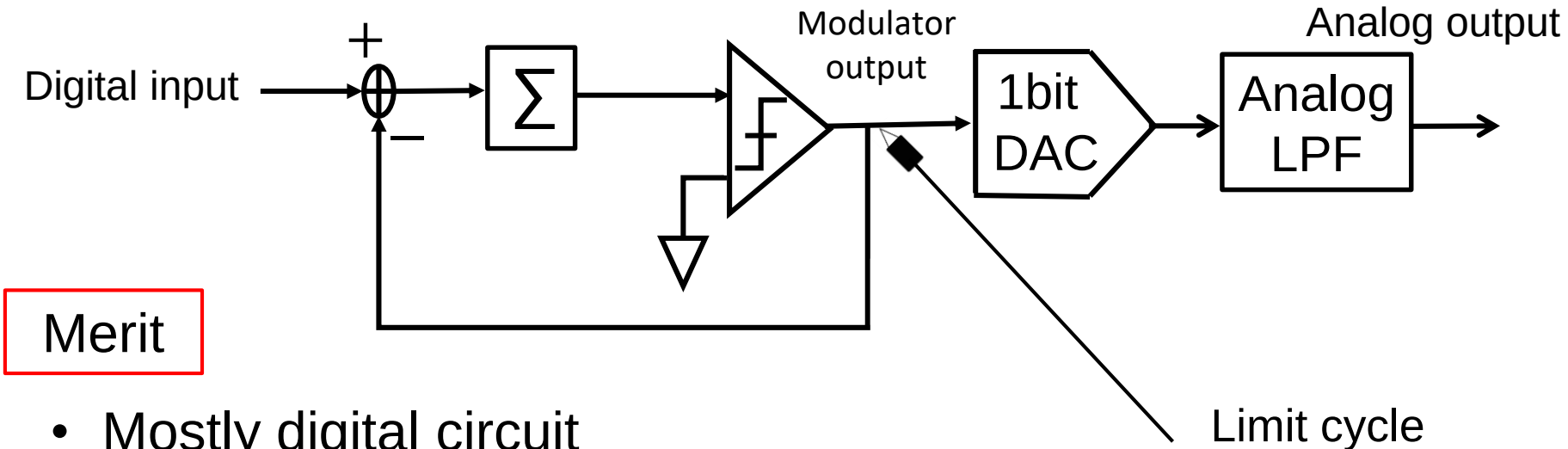
(4) multi-BP type I



(5) multi-BP type II



Merits & Demerits of ΔΣ DAC

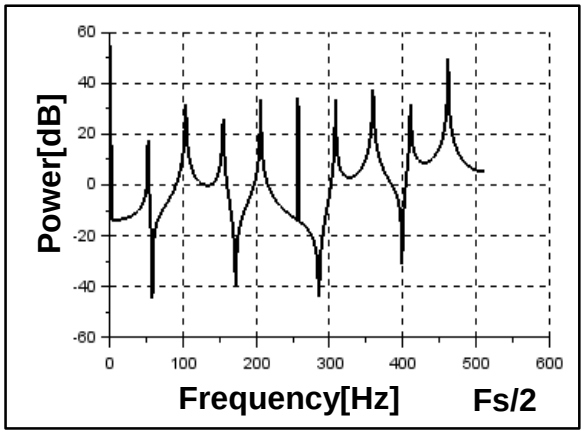


Merit

- Mostly digital circuit
- High linear & high resolution for low frequency signal generation

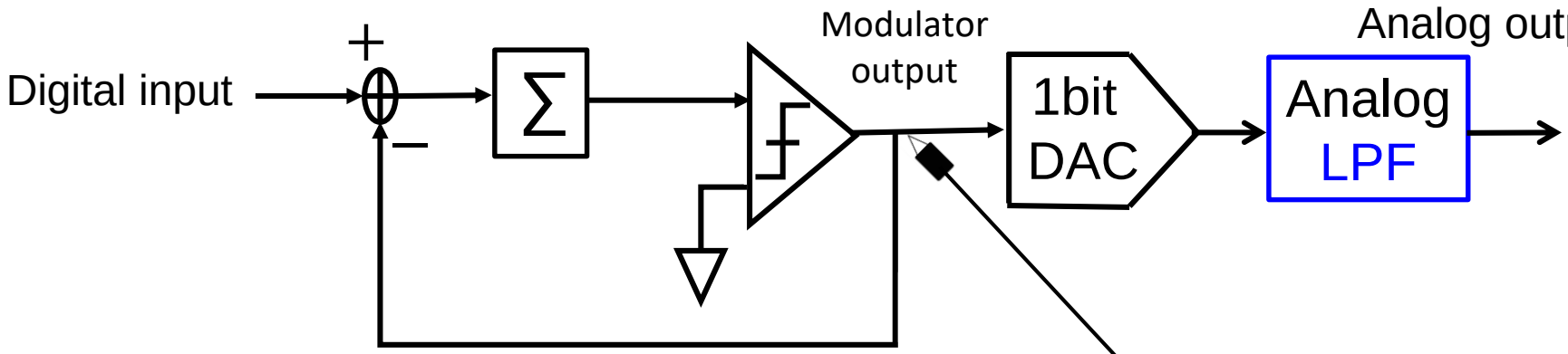
Demerit

- Limit cycle problem for small input



※ Due to modulator nonlinearity by quantizer

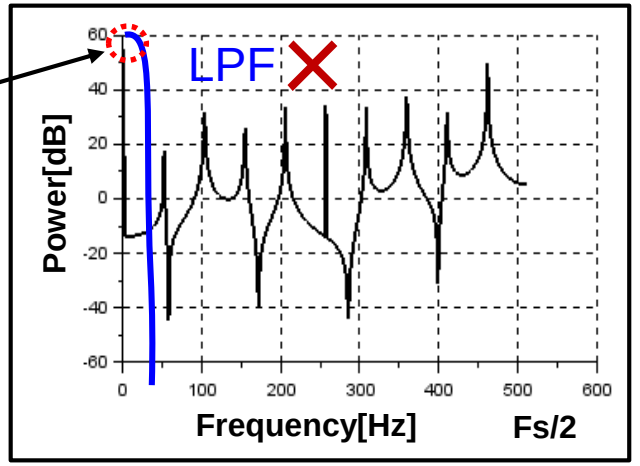
Limit Cycle Problem



Removal of analog signal by LPF sharply

⇒ difficult

Limit cycle



Analog output = Signal + Limit cycle (Noise)

Objective
- Limit cycle suppression
- Relax LPF requirement

Our Studies

Digital input

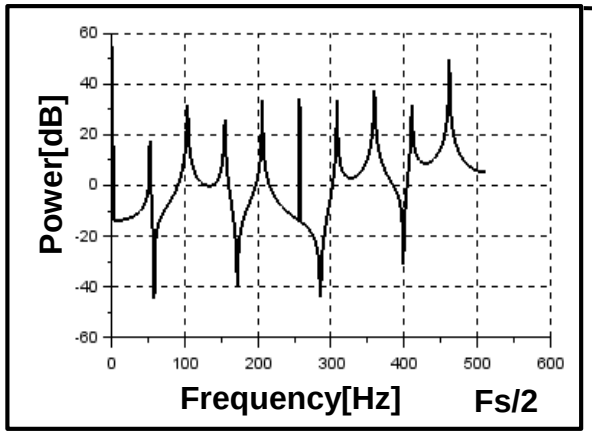
Analog output

Random signal

1bit DAC

Analog LPF

Limit cycle reduction with random signal at quantizer input



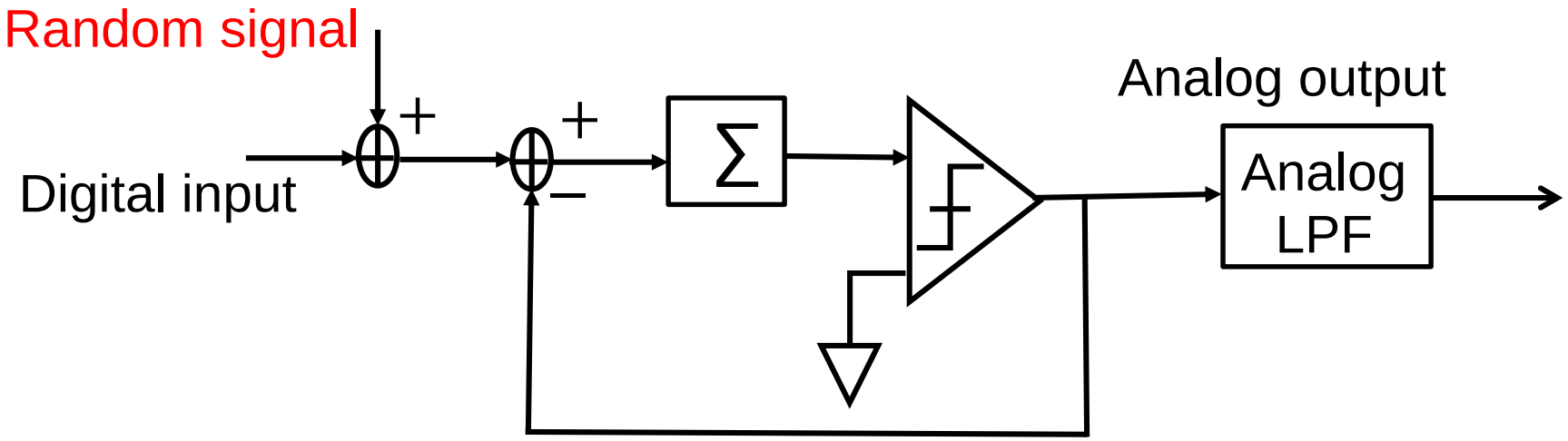
Limit cycle

Stair

Smoothness !

Other Dither Method

Adding random signal to digital input



Drawbacks

- Input range sacrifice
- Random signal has to be out of signal band

⇒ difficult to generate

Outline

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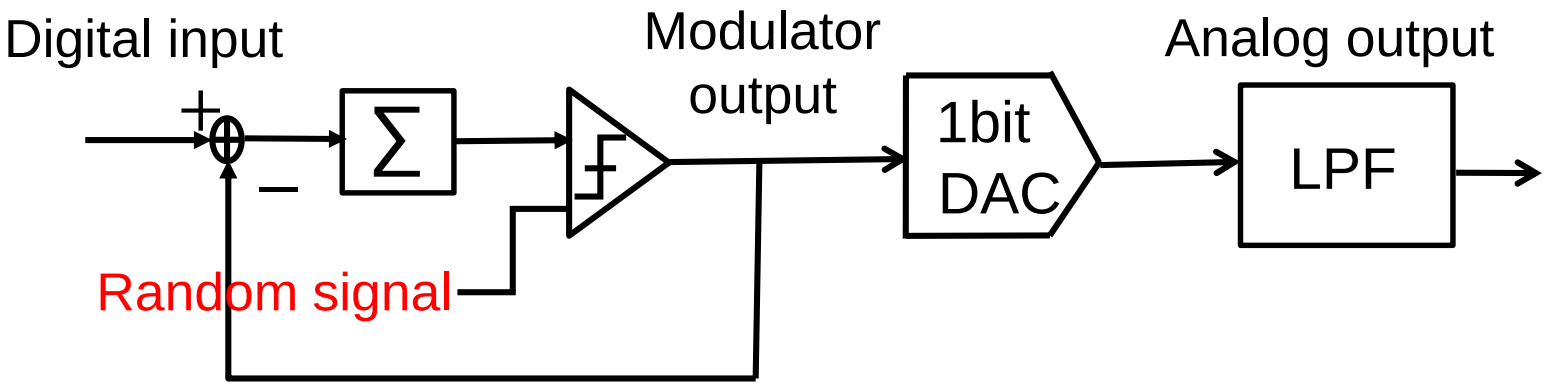
Proposed Method



< Features >

① NOT sacrifice input range

② NOT affect signal band, thanks to noise-shaping

③ Easily generate random signal.

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Simulation Configuration

◆ In 10-bit case

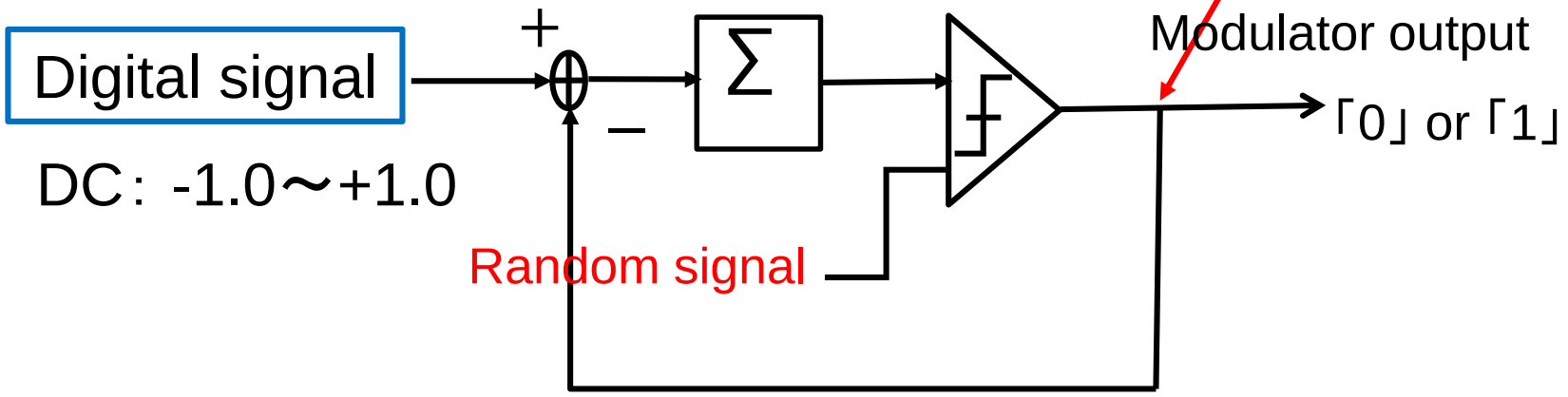
Random signal

Digital dither signal

Controlled by number of 1's

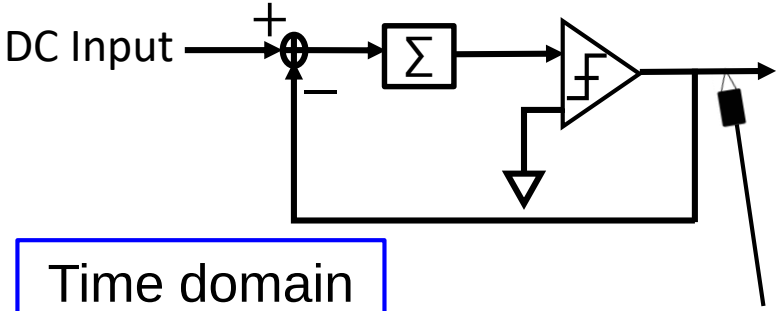
Random signal:

-1.0~+1.0,-2.0~+2.0,-3.0~+3.0



Modulator Operation with Random Signal

- Without random signal

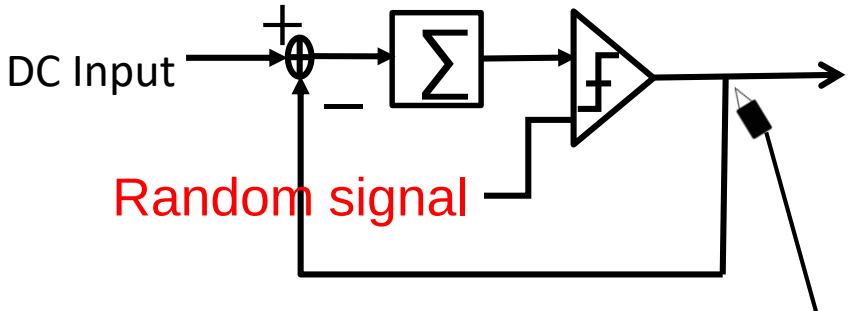


Time domain

1 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0

Period

- With random signal



1 0 0 0 0 1 0 1 0 0 0 0 0 1 0 0

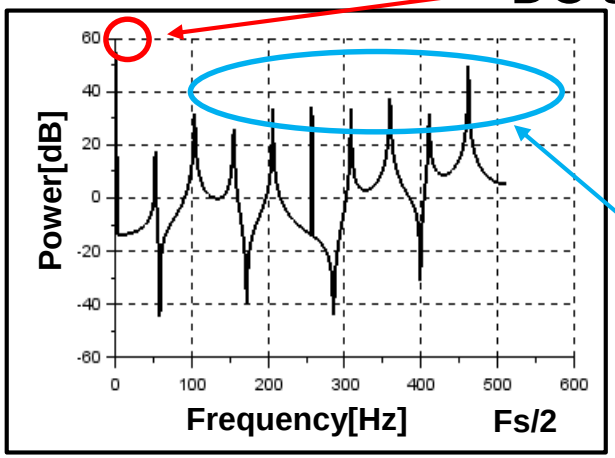
Not Periodic

✓ Orders of ‘0’ and ‘1’ ⇒ different

✓ Total numbers of 1’s ⇒ the same

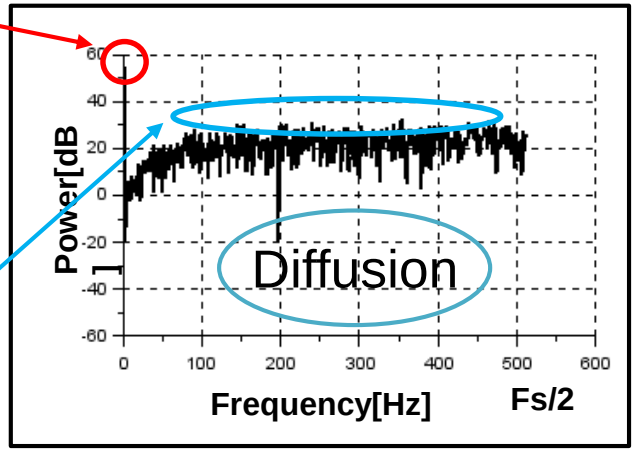
Frequency domain

DC signal power ⇒ the same



Linear

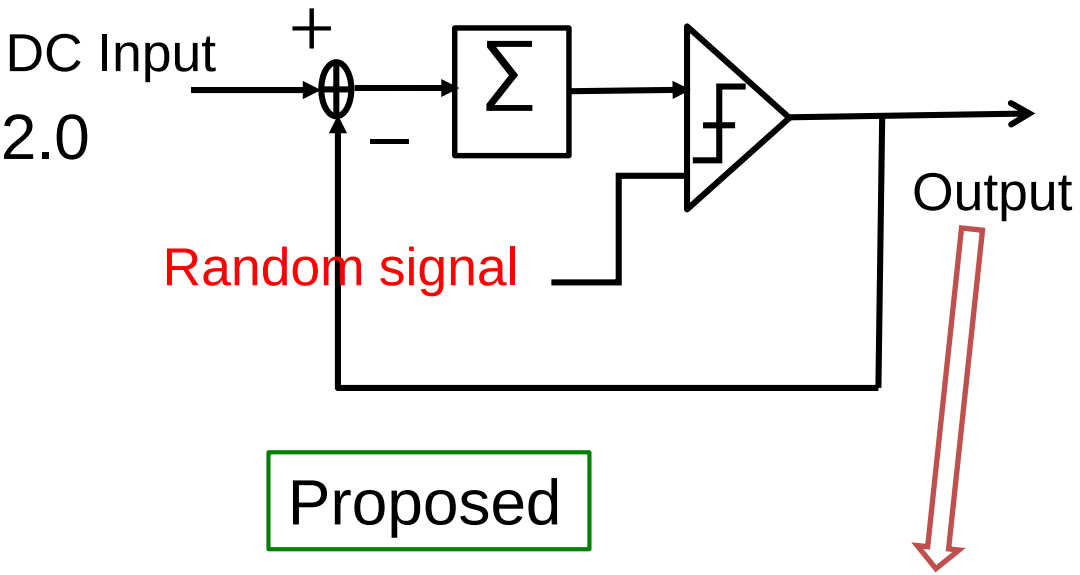
Noise



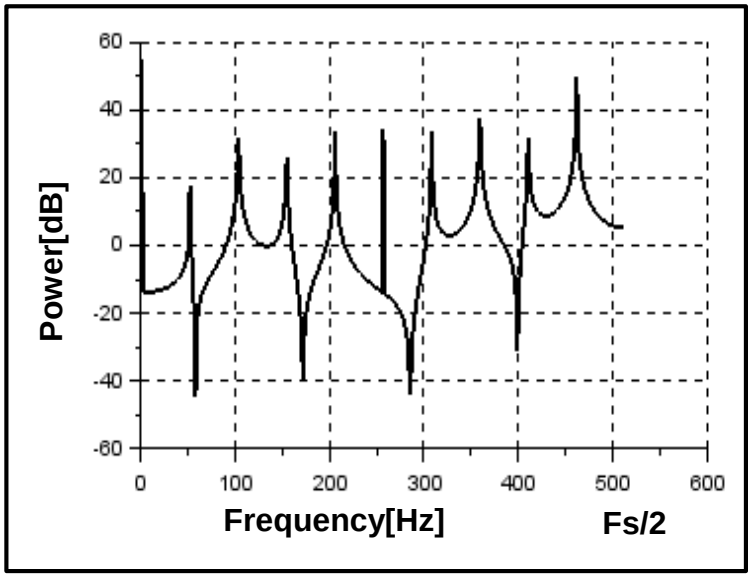
Simulation Results

Random signal : -2.0 ~ +2.0

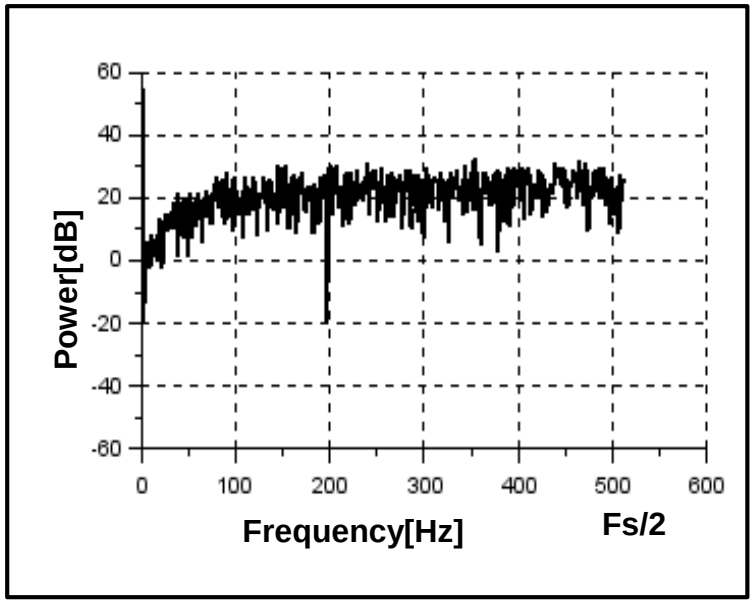
DC Input = 0.1



Without dither



Proposed



SFDR (Spurious Free Dynamic Range)

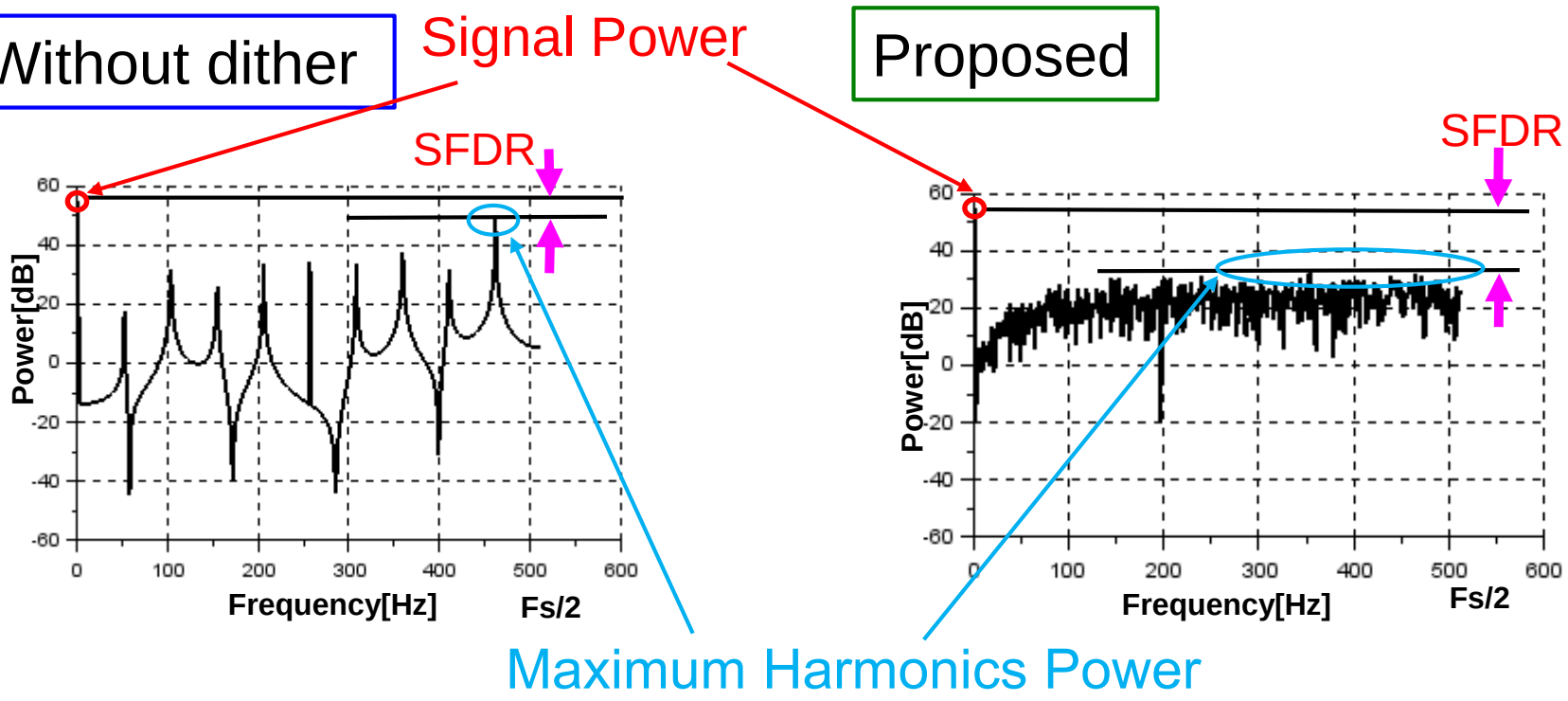
10-bit first-order
LP case
DC = 0.1

$$SFDR = \frac{\text{Signal Power}}{\text{Maximum Harmonics Power}}$$

SFDR = 5.39 dB < 15.59 dB

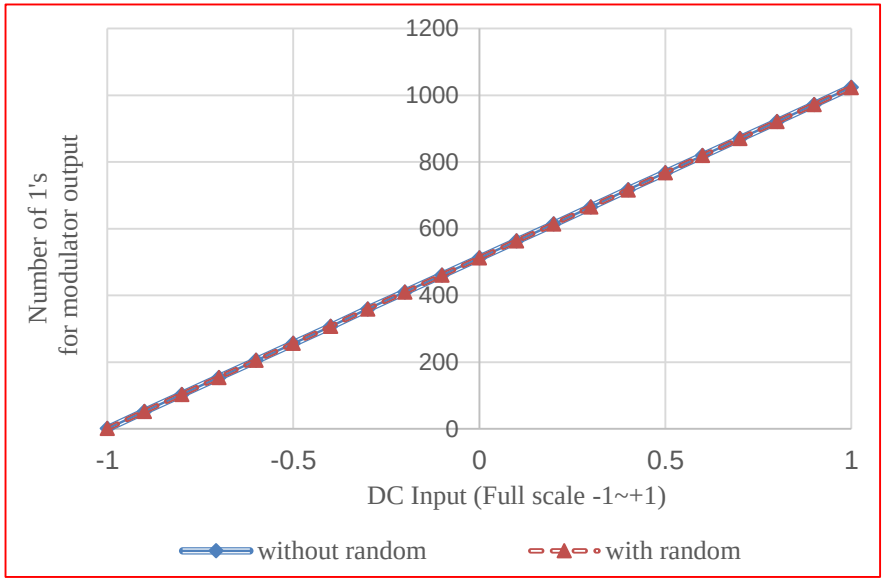
Without dither

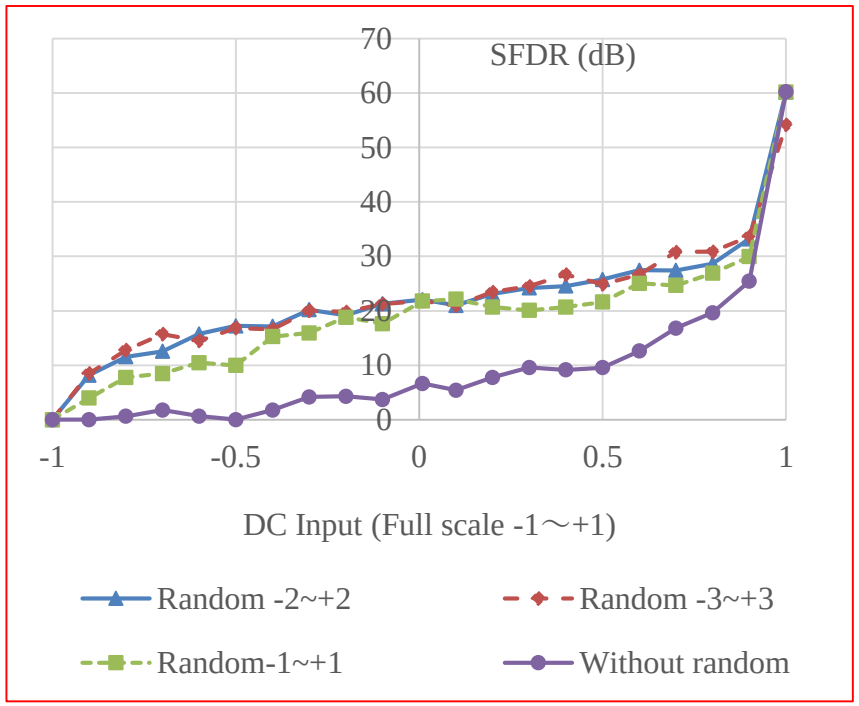
Proposed



SFDR Comparison

Linearity is confirmed
with simulation result.

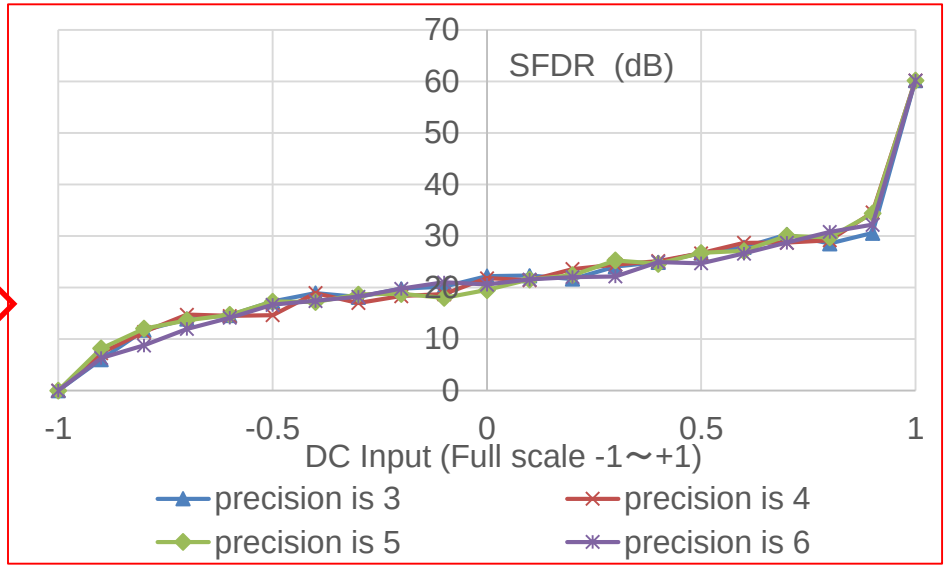


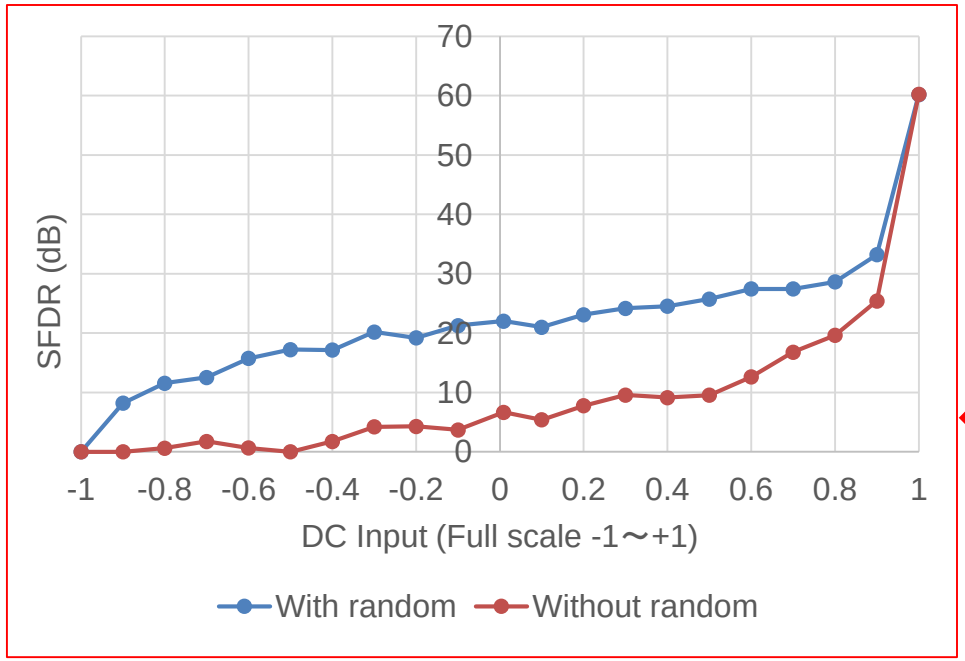


Ideal result can be obtained
with random signal
between -2.0 ~ +2.0

SFDR Comparison

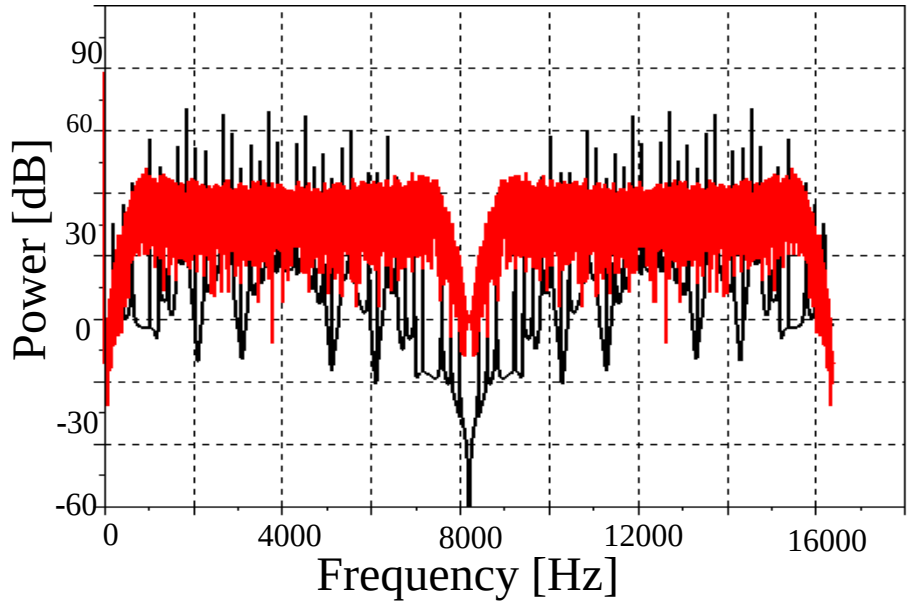
“precision 3” ➡ 1.782
“precision 4” ➡ 1.7824
“precision 5” ➡ 1.78245





SFDR ➡ much improved

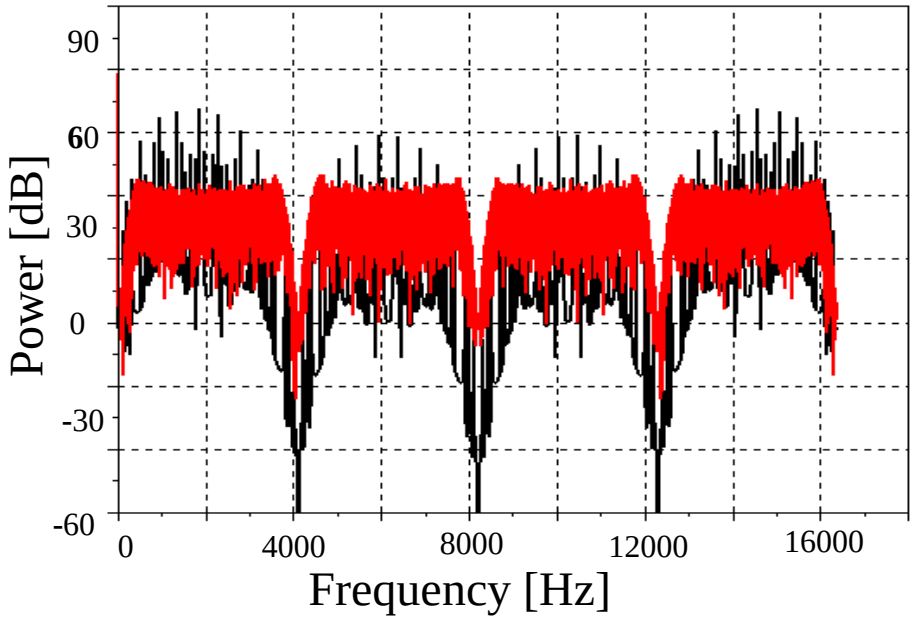
Simulation Results



2–band BP modulator

Red ➡ Spectrum with random signal.

Black ➡ Spectrum without random signal.

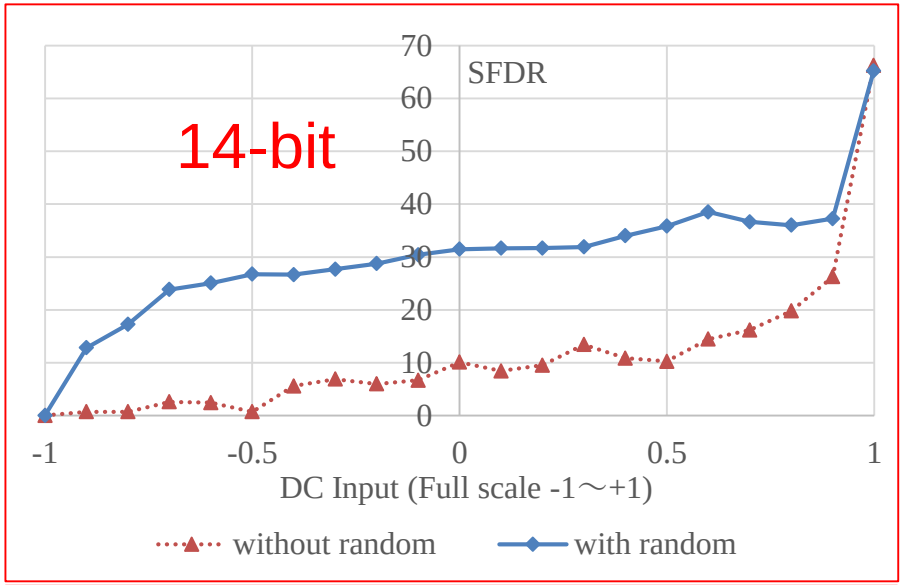


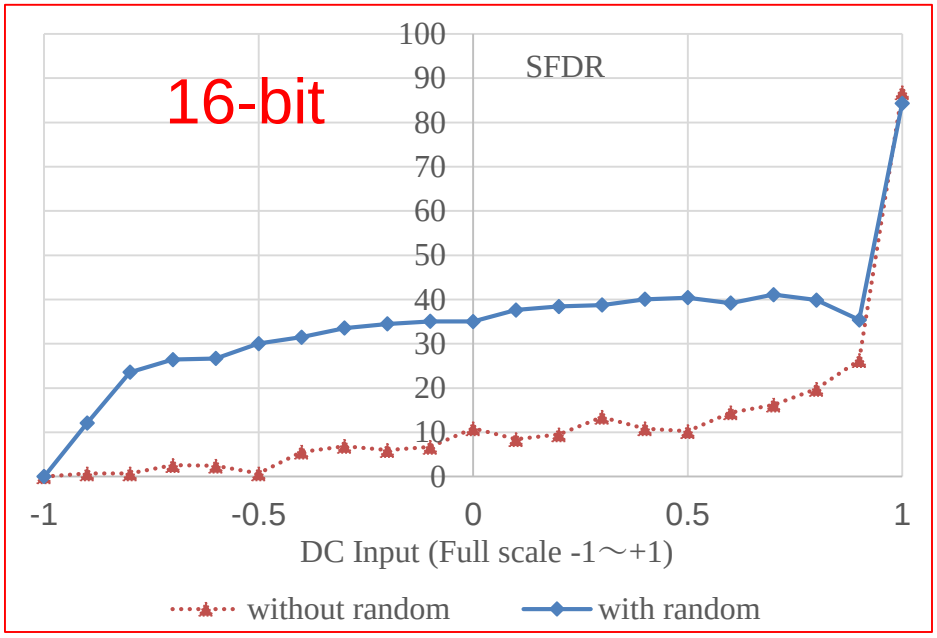
4–band BP modulator

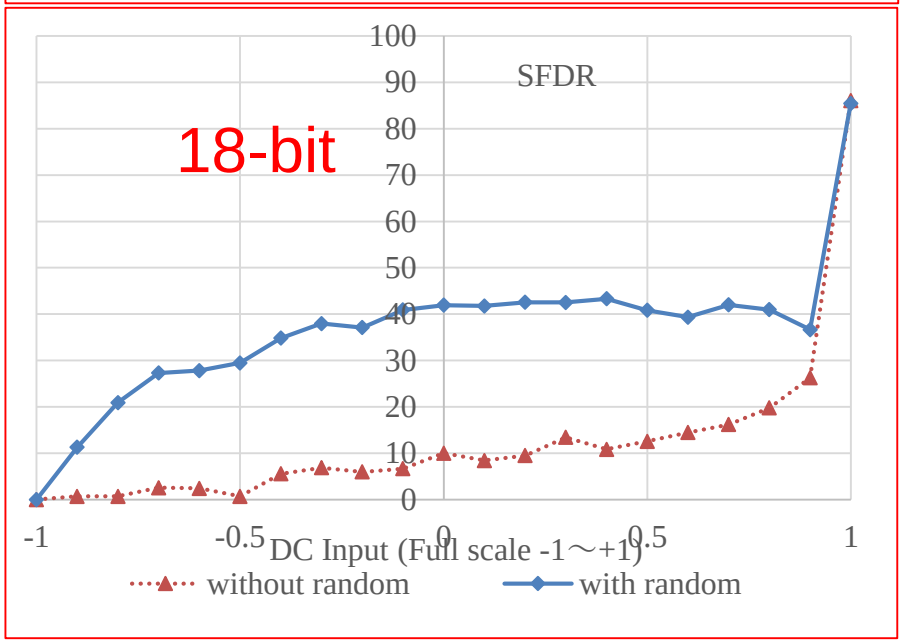
SFDR Comparison

Red line ⇒ without random signal.

Blue line ⇒ with random signal.







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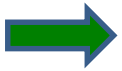
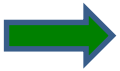
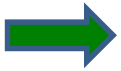
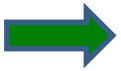
Conclusion

< ΔΣ DA modulator >

Conventional : Limit cycle problem for small input

Proposed : Using random signal at quantizer input

- Limit cycle  reduced
- SFDR much  improved
- Overall linearity of ΔΣ DA modulator  maintained.
- Above statements  valid
  for all LP, HP, BP, multi-BP type modulators.

Thanks for listening！